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Design of 4-Bit Pipeline ADC using Switch Capacitor Circuit in 0.25µm CMOS Technology at 2.5 V

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Abstract: A 4-bit pipeline Analog-to-digital Converter (ADC) is designed using switched capacitor circuit. ADC is designed in 3 stages, 1.5 bit/stage pipeline is used in first two stages and third stage uses two bit flash ADC. The ADC is designed on 0.25 µm CMOS technology at 2.5 V supply voltage in Tanner EDA tool. S/H is used in first stages that consume most of the power consumed by the ADC, after first stage S/H circuit is removed, and also the scaling is used to reduce the power consumption. Cascode opamp is designed with gain of 72.52 dB, phase margin of 66º and unity gain bandwidth of 162.61MHz. The ADC is designed at sampling rate of 5 MS/s and consumes 158.1208 mW powers.

Keywords: Analog-to-digital conversion (ADC), capacitor sharing, opamp sharing, switched capacitor, pipeline ADC, Non overlapping clock.

I. INTRODUCTION

Analog to digital and digital to analog converters are the bridge between the analog world and digital world. Natural signals are analog in nature but better signal processing in digital domain forces to convert analog signal to digital signal. Noise and device limitation limits the bandwidth of analog circuits, also its complex analysis makes design complex. Basic concept of analog to digital converter is shown in the Fig. 1.

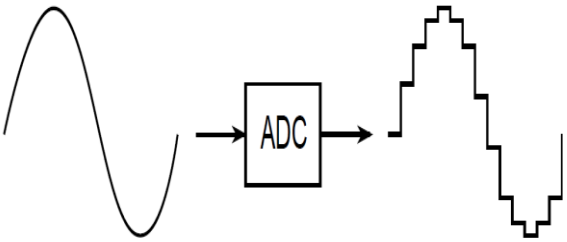

Fig.1 Basic concept of an analog to digital converter

Pipeline ADCs are high speed ADCs capable of resolving medium to high resolutions. [1] These ADCs converts analog signals into digital signals in many stages, each stage converts a portion of input signal to output resolution. The output of first stage is most significant bits (MSB) and the subsequent stages convert LSB bits until the least significant bits (LSB) are converted.

The general architecture of a pipeline ADC is shown in Figure 3.12. Each stage has a similar structure, shown exploded in Figure 3.12. Each block contains a sample and hold block to sample the analog signal. Each stage has its own small flash converter that resolves n-bits. This n-bit output is fed back through a DAC and the converted binary output of sub ADC is subtracted from the original input signal thatgenerates a residue voltage.

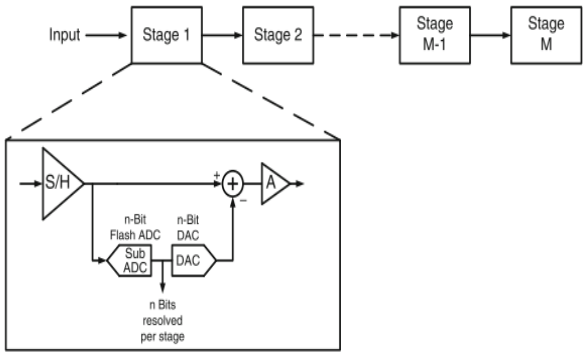

Fig. 2. General Pipeline ADC Architecture [1]

Fig.3. shows a common implementation of a pipeline ADC stage. Typically, the DAC, summer, gain stage and sample and hold are implemented together in one block called a multiplying digital-to-analog converter (MDAC).

The residue voltage is amplified and input into the next stage of the pipeline until the desired number of bits has been resolved.

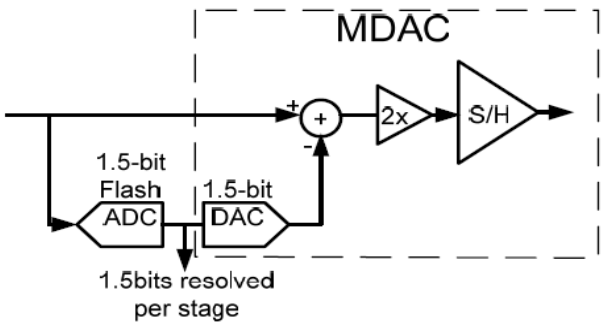

Fig.3. Pipeline stage with MDAC [2]

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II. 1.5 BITS/STAGE PIPELINE ADC

Fig.4. shows the transfer function of a 1.5-bit MDAC that applies DEC. A 1.5-bit sub-ADC quantizes the input to 3-levels and the residue is limited to half the full-scale range. If comparator threshold offsets forces the residue signal to fall outside normal range, the residue signal will be accurately passed into the next stage provided the offset is within $\pm V_{ref} / 4$. Fig.5. demonstrates this by showing the transfer function of a 1.5-bit MDAC when there are threshold offsets in the sub-ADC. The fourth level is removed because the MDAC only needs to indicate whether the residue output is above or below $V_{ref} / 2$ and therefore, there is only an overlap of half bit. The accuracy of the 1.5-bit sub-ADC reduces from N bit to 2 bits using DEC. Generally, by using DEC, the accuracy of the sub-ADC can be increase if fewer bits are resolved in each stage.

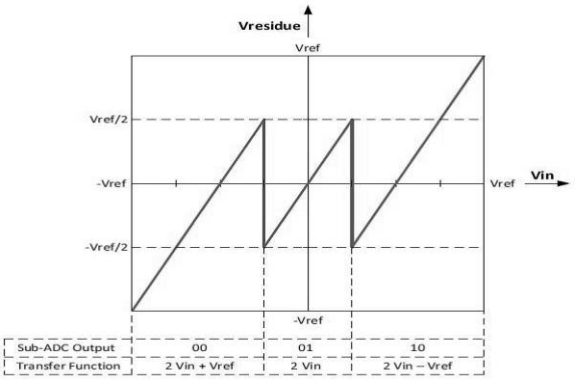

Fig. 4. Transfer function of 1.5-bit MDAC [12]

The pipeline ADC applies DEC and consists of a front-end S/H, 8 pipeline stages, and a 2-bit flash ADC in last stage. Each pipeline stage resolves 1.5 bits/stage, which is represented by a 2 output lines of single bit. In the end, a total of 18-bits are generated from a single input sample. To apply DEC, the bits from each adjacent pipeline stage overlap by half a bit and form the expected 4-bit output.

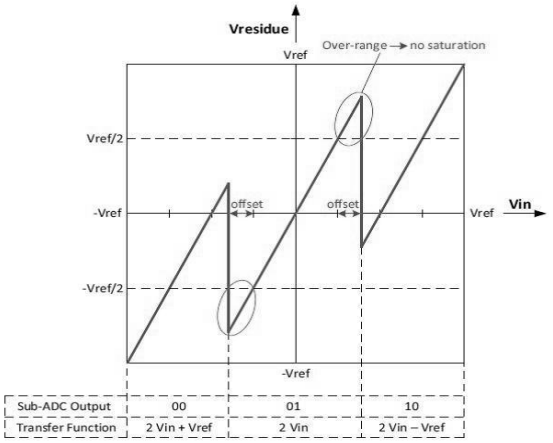

Fig. 5.Transfer function of a 1.5-bit MDAC with comparator offset[12]

III. OPAMP DESIGN

The opamp is used in the MDAC for the gain stage. It's configured in a closed-loop circuit where the closed-loop gain is equal to the stage gain. The three opamp design parameters that are discussed next are gain, bandwidth, and output swing [27].

The settling accuracy refers to how close the residue output settles to its intended value and therefore, it can limit the accuracy of the ADC. Assuming the opamp has sufficient time to settle to its final value, the opamp's open-loop gain, A, sets the settling accuracy. This is because a higher open-loop gain results in a more accurate stage gain and in turn, the residue output follows a more accurate transfer function. To ensure the residue settles to with ΔLSB, the loop gain of the closed-loop, $A\beta$, must be:

$$A\beta > \frac{2^N}{\Delta}$$

Where β is the feedback factor of the closed-loop circuit and $1LSB = \frac{1}{2^N}$. The loop gain, as the name suggests, is the gain around the opamp closed-loop circuit. Considering there are other sources of error (e.g. thermal noise), a reasonable choice is $\Delta = 0.25LSB$. For instance, the front-end sample and hold and first pipeline stage in a 4-bit pipeline ADC requires a loop gain of :

$$\frac{2^{10}}{0.25} = 4096$$

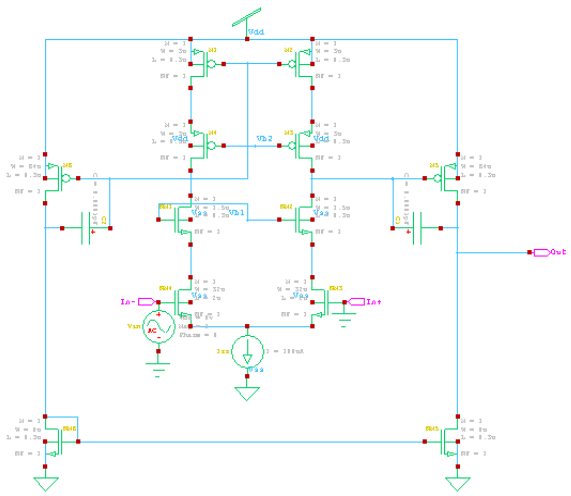

Fig.6. Schematic of Opamp[27]

Assuming the opamp has sufficient gain to accurately settle to its final value, the opamp speed, which determines how fast the residue output settles to a final value, sets the settling accuracy. The bandwidth must be high enough for the opamp to settle to a sufficiently accurate value within the required time of half a sampling period, $0.5 / f_s$

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opamp bias circuits are required to provide a cascode bias to each opamp. Bias voltages for cascade opamp are designed by using the wide-swing cascode current mirrors [3]. A small amount of current scaling is used in this design so as to provide a continuous power scaleable range. As such the bias circuit must keep M2 and M3 in Figure 4.2 in the active region regardless of the bias current (and thus level of channel inversion).

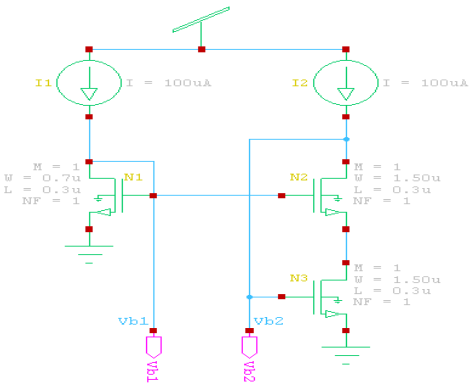

Fig.7. Bias circuit for Opamp[27]

Opamp Gain and phase plot is shown in the Fig. 8.

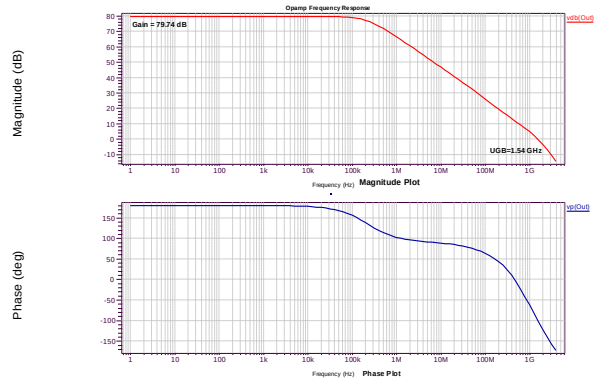

Fig.8. (a) Gain Plot of Opamp (b) Phase Plot of Opa-amp

IV. SAMPLE AND HOLD

The Sample and Hold located at the front of the pipeline performs the first step of sampling the external input signal. Figure 4.7 shows the Sample and Hold circuit used in this ADC. ϕ_1 and ϕ_2 are the clock phase for sample and hold respectively. The total input sampling capacitance the external source must drive in ϕ_1 is $C_{iT,S/H} = C_S$. In ϕ_2, the sample and hold drives a load capacitance to hold the sampled voltage for the pipeline stage. The capacitance C_S does not load the opamp because it's top plate has no path ground. As a result, the feedback factor of the sample and hold is:

$$\beta_{S/H} = \frac{C_S}{C_S + 0} = 1$$

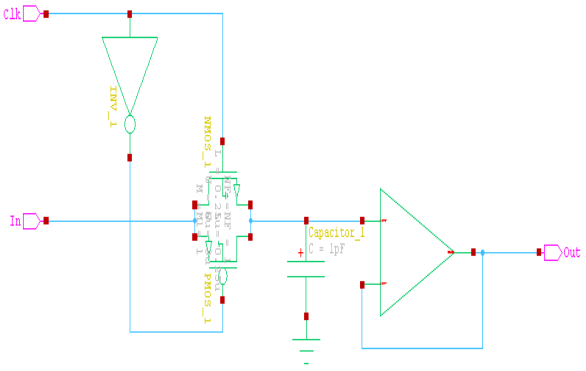

Fig.9. Sample and Hold Circuit[28]

However, the total input sampling capacitance of the sub-ADC, $C_{iT,subADC}$, and of the MDAC, $C_{iT,MDAC}$, in the next stage does load the sample and hold opamp. The opamp is also loaded by an additional capacitance, C_{n2}. The total output load on the sample and hold opamp is:

$$C_{L,S/H} = C_{iT,subADC} + C_{iT,nextstageMDAC} + C_{n2}$$

From [17], the differential input-referred thermal noise power of a sample and hold or an MDAC is:

$$\overline{v_{i/p}}^2 = \left(2\frac{kT}{C_S} + \frac{4}{3}\frac{kT}{C_c}\beta(1+n_f) \right)$$

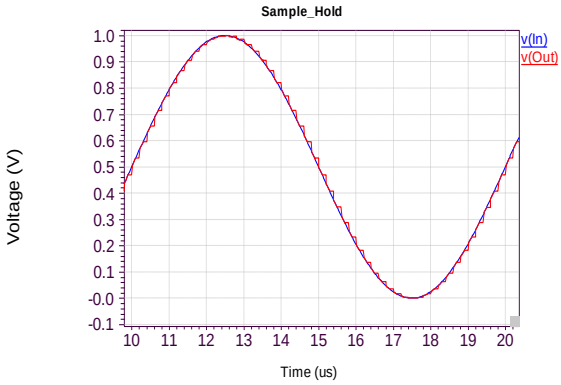

Fig.10. Transient response of Sample and Hold circuit

Where C_c is the compensation capacitor used to stabilize the opamp closed-loop circuit. As the input signal is being sampled in ϕ_1, thermal noise from the transistor is sampled across C_S.

The opamp is not used and therefore, does not contribute any noise. The dominate sourse of noise is from the Op-amp's first stage, the noise from the second stage is negligible because, once input-referred, it is greatly reduced by the gain of the opamp. The noise fraction, n_f, defined in equation 4.12. The formula is based on a similar calculation performed on a simple opamp in [18].

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$n_f = \frac{g_{m3} + g_{m9}}{g_{m1}}$ Since typically n_f =1 and $\beta_{S/H}$ =1, the input referred thermal noise power of the S/H block is

$$\overline{v_{i/p,S/H}}^2 = \left(2\frac{kT}{C_S} + \frac{4}{3}\frac{kT}{C_C} \right)$$

V. MDAC DESIGN

Since 1.5 bits/stage architecture has one of three digital outputs, thus the DAC has three operating modes.

ADC output=01: No over range error (stage input is between $-\frac{V_{ref}}{4}$ and $+\frac{V_{ref}}{4}$).During ϕ_1 : $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$ During ϕ_2 : C_1 is discharged, thus by charge conservation: $C_1 V_{in} + C_2 V_{in} = C_2 V_{out}$ (noting negative feedback forces node V_p to a virtual ground)Thus $V_{out} = \frac{C_1 + C_2}{C_2} V_{in} \rightarrow if C_1 = C_2, then: V_{out} = 2V_{in}$

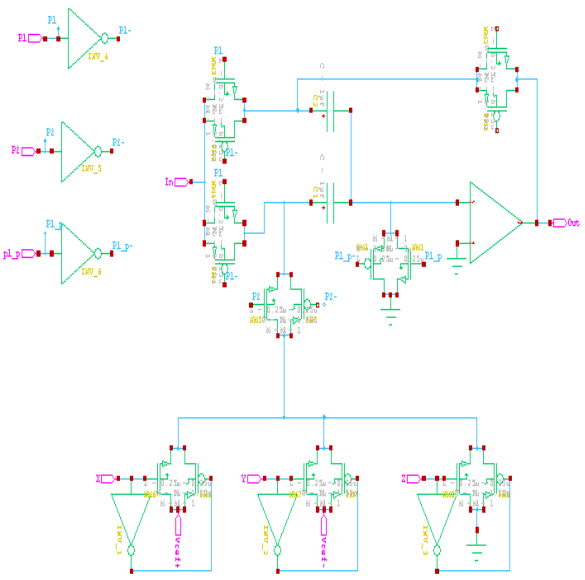

Fig.11. Multiplying Digital to analog converter [10]

ADC output=10: Over range error-Input exceeds $+\frac{V_{ref}}{4}$, thus subtract $\frac{V_{ref}}{2}$ from input during ϕ_1 : $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$

During ϕ_2 : C_1 is charged to V_{ref}, thus by charge conservation $C_1 V_{in} + C_2 V_{in} = C_1 V_{ref} + C_2 V_{out}$

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} V_{in} - \frac{C_1}{C_2} V_{ref} \rightarrow if, C_1 = C_2, then: V_{out} = 2V_{in} - V_{ref} = 2(V_{in} - V_{ref}/2)$$

ADC output=00: Under range error-Input below $-\frac{V_{ref}}{4}$, thus add $\frac{V_{ref}}{2}$ to input During ϕ_1 : $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$ During ϕ_2 : C_1 is charged to $-V_{ref}$. Thus by charge conservation

$$C_1 V_{in} + C_2 V_{in} = C_1(-V_{ref}) + C_2 V_{out}$$

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} V_{in} + \frac{C_1}{C_2} V_{ref} \rightarrow if, C_1 = C_2, then: V_{out} = 2V_{in} + V_{ref} = 2(V_{in} + V_{ref}/2)$$

Thus the switched capacitor circuit can be used to implement the sample-and-hold, gain stage, DAC, and subtraction blocks of ADC. To reduce the signal dependent charge injection bottom plate sampling technique is where the use of an advanced clock ϕ_{1p} , makes charge injection signal independent [10]. The total input sampling capacitance in ϕ_1 is $C_{iT,MDAC} = C_1$. In ϕ_2 , the two $C_1/2$ capacitors apply a load of $C_1/4$ on the MDAC opamp. Taking into consideration the loading effects of the next stage and of the parasitic capacitance C_{n2} , the total output load on the MDAC opamp is:

$$C_{L,flipMDAC} = C_1/4 + C_{iT,subADC} + C_{iT,nextstageMDAC} + C_{n2}$$

The feedback factor of MDAC is:

$$\beta_{MDAC} = \frac{C_1/2}{C_1/2 + C_1/2} = \frac{1}{2}$$

The differential input-referred noise of MDAC is:

$$\overline{v_{i/p,MDAC}}^2 = \left(2\frac{kT}{C_1} + \frac{4}{3}\frac{kT}{C_2}\left(\frac{1}{2}\right)(2) \right)$$

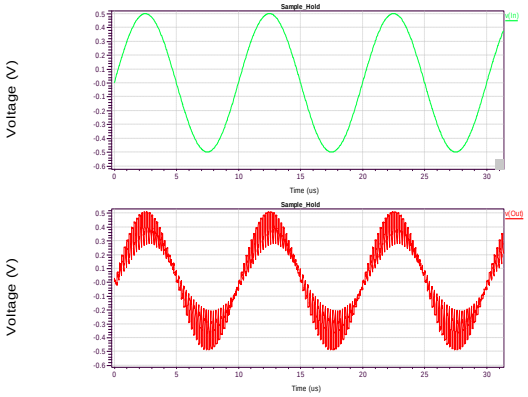

Fig.12. transient response of MDAC for sinusoidal input at 300 kHz, 0.5 V

VI. NON OVERLAPPING CLOCK GENERATOR

Non-overlapping clocks are required in the MDAC to minimize the effect of signal-dependent charge injection. Non-overlapping clocks were generated using the design of Figure 5.11, where the non-overlap time is given by the minimum delay of t_2 and $t_2+t_3+t_5$.

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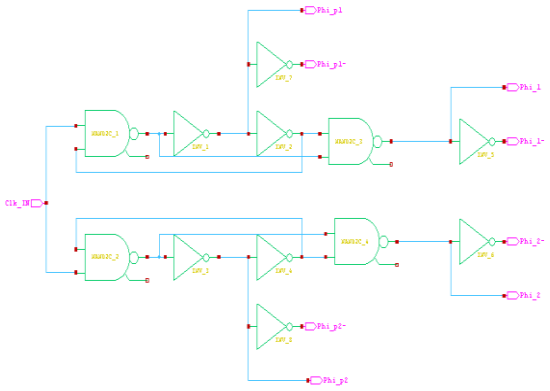

Fig.13. Non-Overlapping Clock generator circuit [33]

For this design, to improve the likelihood of design functionality a longer non-overlap time has been favoured.

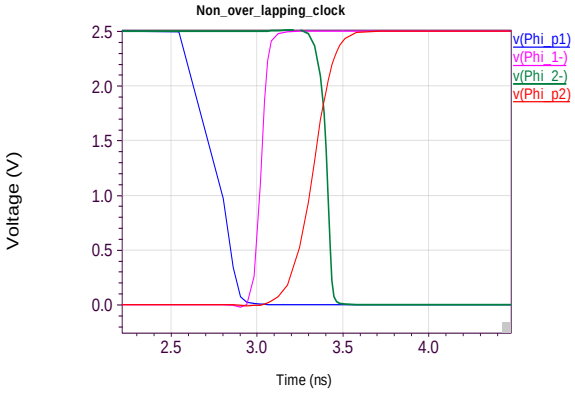

Fig.14. Non-Overlapping Clock

VII. COMPARATOR

Comparator used in this paper consists of three stages: the input preamplifier, output buffer stage and decision stage. The preamplifier section improvise the sensitivity of comparator to input signal by amplifying the input signal, it also isolates from the switching noise emerging from the positive feedback. The positive feedback stage increases the gain and produces an output to decide which of the input signals is larger. The output buffer also provides some gain and couples it to the other digital circuits.
Schematic of pre-amplification stage is shown in Fig. 15; This circuit is differential amplifier with active loads. The sizes of M6 and M7 are set by considering the differential amplifier trans-conductance, g_m , and input capacitance. The trans-conductance of M1 and M2 decides the gain of the stage, while M6 and M7 determines the input capacitance of the comparator.
Transistor M9 amd M8 are used as current mirror to bias the preamplifier stage at bias current of 12 µA. transistor M1 and M4 are active load to the preamplifier stage. This is to ensure high speed. The relation between input voltages and output current i_o is given by

$$i_o = \frac{g_m}{2}(V_p - V_n) + \frac{I_{ss}}{2}$$

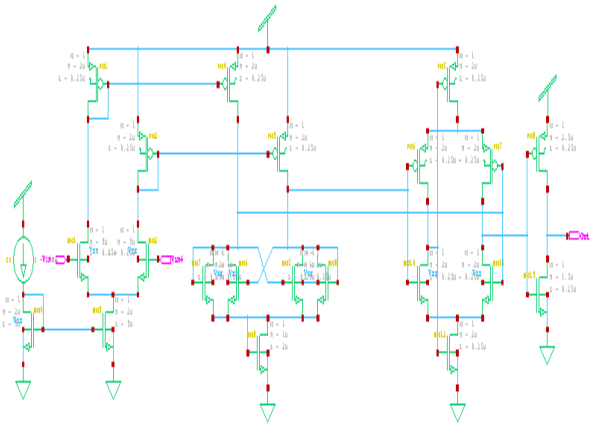

Fig.15. Schematic of Comparator

The decision circuit is the important section of comparator that can discriminates mV level signals. The circuit used in the comparator is shown in Figure 4.4 which uses positive feedback from the cross-gate connection of M10 and M11 to increase the gain of the decision element.
In this circuit M9 and M12 are identical similarly M10 and M11 are identical. The output voltage of non-inverting terminal is given by

$$V_{op} = \sqrt{\frac{2 i_{op}}{\beta_9}} + V_{THN}$$

VIII. FOUR BIT PIPELINE ADC

The complete schematic of 4-bit pipeline ADC is shown in figure 4.12, First and second stage are identical and sampled capacitor C2 =C1= 1 µF is used. After second stage scaling is done to reduce the power consumption and uses C1=C2=0.5 µF and 0.25 µF for third, fourth stage respectively.

The setup of 4-bit pipeline ADC is shown in Fig.17, for a sinusoidal signal of 5 MHz. And the simulated 4 bit output is shown in the figure 5.9

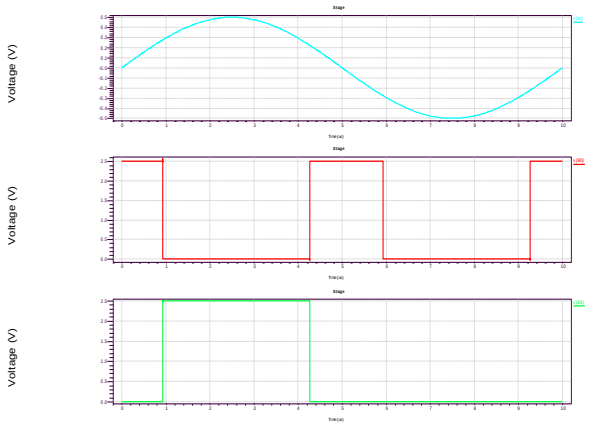

Fig.16. Transient response of 1.5 bit/stage sub ADC

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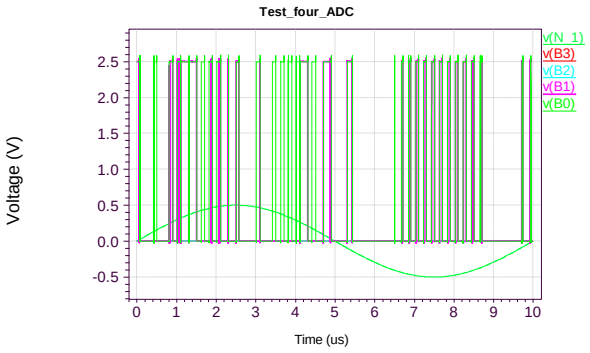

Fig.17 Transient response of 4-bit ADC

IX. PERFORMANCE SUMMARY

Technology	0.25 µm CMOS process
Resolution	4 bit
Supply Voltage	2.5 V
Conversion rate	5 MS/s
Power	78.12mW

X. CONCLUSION

The goal of this paper was to design a 2.5 V, 1.5 bit/stage 4bit ADC by using switched capacitor technique. The ADC is designed in 0.25 µm CMOS process at 2.5 V supply voltage. It also shows the comparison between the power consumption of stages with the S/H and without S/H which gives 28.33 mW in first stage (with S/H) and 19.59 mW third stage (without S/H).Further the ADC is tested at input frequency of 1 MHz and sampling rate of 5 MS/s, at which ADC consumes 78.12mW power.

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